AN ANALOG X-BAND PHASE SHIFTER

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ABSTRACT

A hybrid-coupled phase shifter has been fabricated monolithically using reverse-biased Schottky varactor diodes to continuously vary phase with an analog control voltage. A phase shift of 105° is obtained at X-Band, and with design improvements a phase shift of 180° over the full 8-12.4 GHz is expected. Phase shift variation with power level is reduced by using back-to-back varactors on the direct and coupled ports of the coupler. A six-to-one reduction in size compared to a four-bit switched-line phase shifter (also at X-Band) results from this approach.

INTRODUCTION

The capacitance vs. voltage characteristic of a reverse-biased Schottky diode was used to make a monolithic analog phase shifter at X-Band. A Lange coupler was fabricated on 0.010" thick GaAs along with selectively ion implanted varactors and bias resistors. The circuit (Fig. 1) consists of a back-to-back varactor pair on each port of a 3-dB coupler. The input signal splits and is incident upon the two varactor pairs. Signal reflected from the varactor pairs adds at the output and is varied in phase relative to the input as the diode capacitance is varied by the input as the diode capacitance is varied by the external bias. By adjusting the tuning inductance in series with the diodes, 180° of phase shift over an 8-12.4 GHz bandwidth is possible. The layout and fabricated chip of Figures 2 and 3 show the airbridged Lange coupler formed in a U-shape with the varactors and bias/isolation resistors located in the middle. The varactors are grounded around the edge of the substrate. The resistors are small enough in value to provide a return path for the diode leakage currents, but large enough not to load the RF signal path.

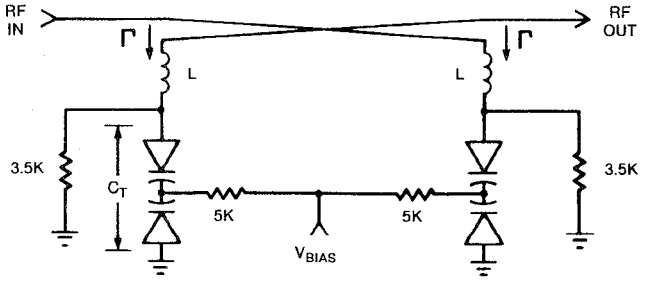

Fig. 1. Hybrid-Coupled Phase Shifter Circuit Uses Back-to-Back Varactors (similiar to VCO circuits).

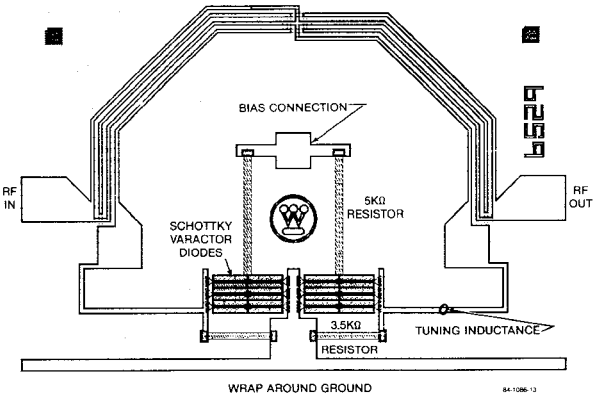

Fig. 2. CAD Chip Layout.

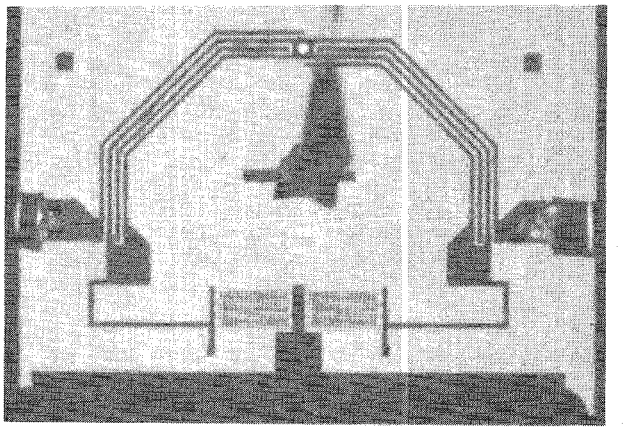

Fig. 3. Chip Size Is 0.077 x 0.100 Inches.

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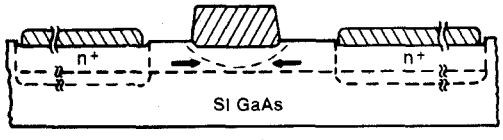
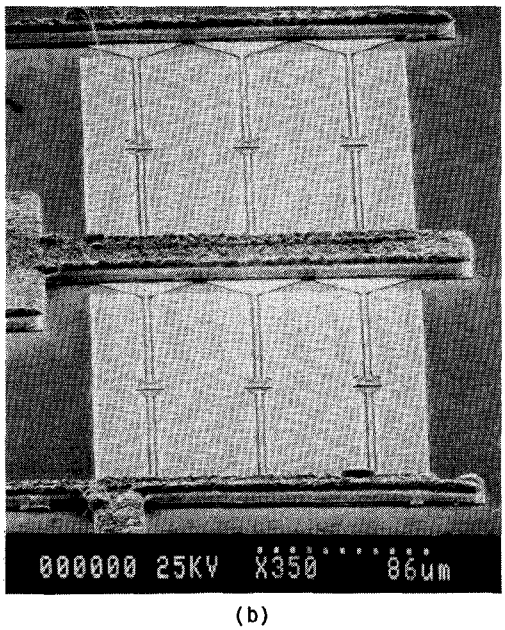
DIODE GEOMETRY AND FABRICATION

Surface oriented diodes made on the same active layer as FETs punchthrough at 2-4 V. as dictated by the FET pinchoff voltage. This gives the maximum range of capacitance. However, as the depletion layer nears pinchoff the diode series resistance increases because lateral current has less active layer through which to flow [1]. A buried N^+ layer can be used [2,3] but it involves more complicated processing. Instead, the approach here has been to make the active layer implantation as deep as possible so that breakdown occurs before punchthrough to allow the conduction layer to completely surround the cathode side of the depletion region and maintain low series resistance (Fig. 4). The doping concentration was chosen to be as high as possible for low series resistance but low enough to insure 80% depletion of the active layer without breakdown in order to achieve the greatest change in capacitance. N^+ contacts implanted deeper than the active layer were desired to provide low resistance from the ohmic contact to the depletion region at all bias levels. However, substrate overheating and photoresist carbonation during implantation limit the deepest practical N^+ implant to 0.6 microns, and therefore an active layer thickness of 0.5 microns was chosen.



(a)



(b)

Fig. 4. (a) Diode Cross-Section illustrates restricted lateral current flow through undepleted active layer near punchthrough. Anode-N^+ spacing is 1.0 micron; anode width is 1.5 microns. (b) SEM Photo shows the four varactors each consisting of three 135 micron anode fingers in parallel.

The active and N^+ layers have been selectively implanted into LEC semi-insulating substrates (4000 - 5000 cm^2/V-sec mobility) with the implant schedule of Table I and capless annealed at 750°C. A concentration of 9 x 10^{16} cm^{-3} and a mobility of 3000 cm^2/V-sec are obtained. The active layer depth (LSS theory) of 0.4 microns increased to 0.5 microns after annealing. The diode (edge) breakdown is 10 V.; bulk breakdown for 10^{17} cm^{-3} material is 15 V. The depletion depth at 10 V. is 0.4 microns and punchthrough does not occur.

The circuit layout has been carefully designed for optimum use of chip area while minimizing cross-coupling effects. A value of 300 ohms/square was used for the implanted resistor design and gave a feasible and easy to implement resistor layout for the values needed. The Lange coupler uses six airbridges and is folded to reduce overall chip size. The input/output VSWRs are less than 1.5:1 indicating that the bends had minimal affect on the coupler performance. The placement of the wrap around ground minimizes parasitic inductance to ground. Only one additional bond is required for biasing the four diodes. A high yield design results from the elimination of sub-micron linewidths and relatively thin active layers. The anode width of 1.5 microns can be repeatably defined with standard optical lithography. Variations in anode width across a wafer causing variations in phase shift between chips can be corrected by adjusting the bias appropriately.

Table I. Implant Schedule.

N^+ Implant Schedule

$^{28}Si^{++}$	2.42 E13/cm^2	500 KeV
$^{28}Si^{+}$	1.50 E13/cm^2	240 KeV
$^{28}Si^{+}$	7.00 E12/cm^2	100 KeV
$^{28}Si^{+}$	2.57 E12/cm^2	60 KeV

(The GaAs is etched 700 Angstroms prior to implant for a deeper N+ layer and for later aligning).

Active Layer Implant Schedule

$^{28}Si^{+}$	3.51 E12/cm^2	300 KeV
$^{28}Si^{+}$	1.79 E12/cm^2	120 KeV
$^{28}Si^{+}$	5.10 E11/cm^2	60 KeV

Fabrication of the phase shifter utilizes all positive photoresist with a total of seven masking levels. Fig. 5 shows the first five mask levels. The remaining two are for the airbridge formation. All circuit paths are plated to 4 microns of gold to reduce RF losses.

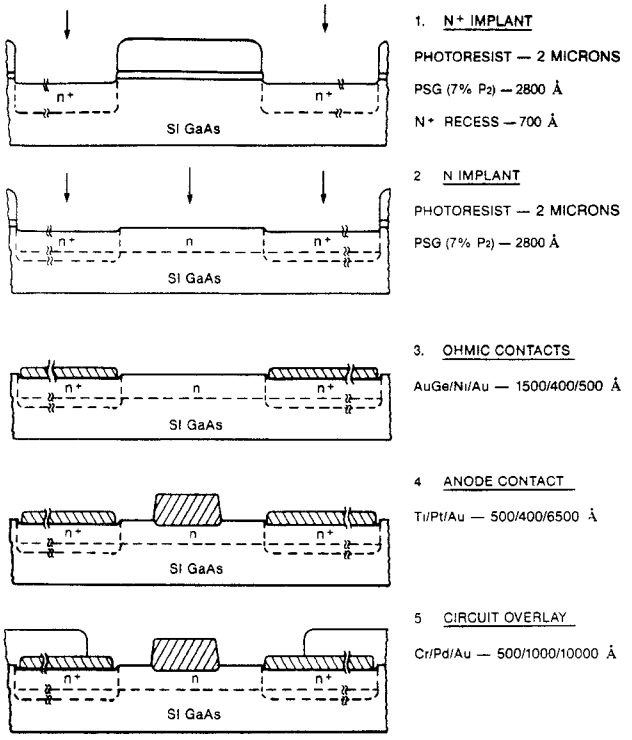


Fig. 5. Selective ion implant, ohmic, anode, and overlay fabrication sequence.

DESCRIPTION OF CIRCUIT DETAILS

The phase shifter configuration makes use of a 3 dB quadrature (Lange) coupler to provide a matched input and output (low VSWR) for the phase shifting elements. Figure 1 shows the hybrid coupler type of phase shifter with series L-C loading elements, where the capacitive element is a series pair of voltage variable (varactor) diodes. Figure 6 is a Smith chart diagram showing the reflection coefficient for various varactor capacitances. A full 180 degree phase change is obtained for a 3:1 capacitance variation. Figure 7 is a plot of the relative phase shift as derived from the Smith chart of Figure 6 where the capacitance values have been related to the bias voltage according to the equation for Schottky barrier (abrupt) junctions; i.e., $C(V) = C(0)/(1-V/\phi)^{1/2}$, where ϕ has been given the two values of 0.8 and 0.9 volts. Notice that this form of phase shifter has a very smooth, well behaved variation of phase as a function of bias voltage. This makes the job of microprocessor control easier, including temperature stabilization.

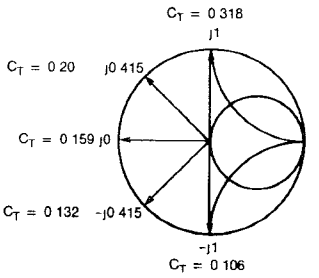


Fig. 6. Phase Shift Varies 180° as C_T varies from $C_T(0)$ = 0.318 pF ($C_j(0)$ = 0.636 pF) to 1/3 the zero-bias value. A frequency of 10 GHz and series inductance of 1.59 nH are assumed.

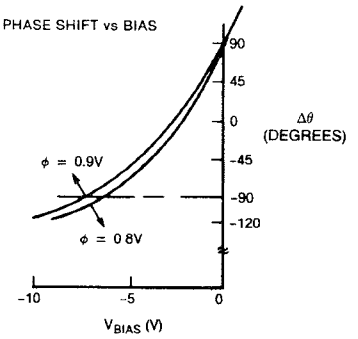


Fig. 7. Phase Shift Varies Smoothly With Bias. Frequency is 10 GHz.

Figure 8 shows the calculated transmission phase characteristics of a single section of the hybrid-coupled phase shifter. The fact that this type of phase shifter does yield a phase change which is relatively independent of frequency can be seen from this figure. Examination of a broader frequency range shows that at least 180° of phase shift can be obtained (for a 0 to 10 volt swing) over the frequency band of 8 to 12.4 GHz.

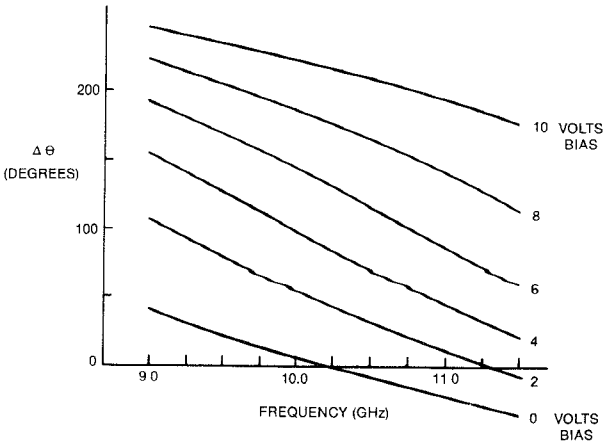


Fig. 8. Calculated Transmission Phase vs. Frequency is smooth, and the step size with bias is also uniform over the frequency band.

The phase shift variation with signal level is greatest for the analog phase shifter at zero bias where the capacitance vs. voltage slope is steepest. The series back-to-back configuration has a compensating effect compared to the single varactor. As the RF swing increases the capacitance of one varactor, the capacitance of the other is decreased. The variation of the total capacitance, C_T, given by $1/C_T = 1/C_1 + 1/C_2$ is of second order. However, if the onset of forward conduction is reached on one of the varactors, the compensating effect becomes out of balance. By being d-c biased in parallel the 3:1 capacitance variation is maintained, but the variation caused by the RF swing is reduced by the back-to-back series connection at RF. A 0.4 V. peak swing applied to a 0.318 pF single varactor causes a capacitance swing with a maximum of 0.449 pF and a minimum of 0.258 pF. The average is 0.354 pF, a 10% increase. With 0.4 V. peak across each of two 0.636 pF varactors back-to-back the maximum capacitance is 0.328 pF, and the minimum is 0.318 pF. The average (allowing for a capacitance swing twice each cycle) is 0.325 pF, a 2% change. Following the Smith chart of Fig. 6, the phase shift variation at zero bias for the 10% change of the single varactor is six degrees, and the back-to-back configuration shifts one degree. In addition, the back-to-back configuration is operating at a 6 dB greater power level because the signal is across two varactors (each of half the impedance) instead of one. Therefore, for a given tolerated phase error, the back-to-back varactors will handle more signal swing or bias closer to zero, or slightly forward, allowing greater phase shift.

The series resistance of the varactor string is measured to be about 3.0 ohms. At series resonance, this gives about 1.0 dB return loss (in a 50 ohm system). If we assume that the Lange coupler plus transmission lines have about 0.6 dB insertion loss per pass, then the phase shifter is expected to have about 2.2 dB insertion loss at resonance. The loss should be slightly less at the +90 & -90 degree and other off-resonance points.

PERFORMANCE

Measured series resistance of a single varactor junction is 1.5 ohms. The zero-bias capacitance was predicted to be 0.636 pF, and the resulting devices have 0.9 pF. The design value was based on a parallel-plate model and did not account for fringing. The C-V characteristics have a 3:1 change in capacitance as expected. The resulting measured phase shift is less than 180^0 because the range of capacitance and tuning inductance were incorrect. A phase shift of 105^0 at 11 GHz was measured (Fig. 9). The calculated results of a revised model of the phase shifter with $C_j(0) = 0.9$ pF and a series tuning inductance of 0.6 nH are shown in Fig. 10. The calculations are in good agreement with the measured phase shift of Figure 9. The measured insertion loss is 2.5 dB and varies ±0.5 dB as the phase is varied from 0^0 to 105^0. The transmission phase versus frequency for different

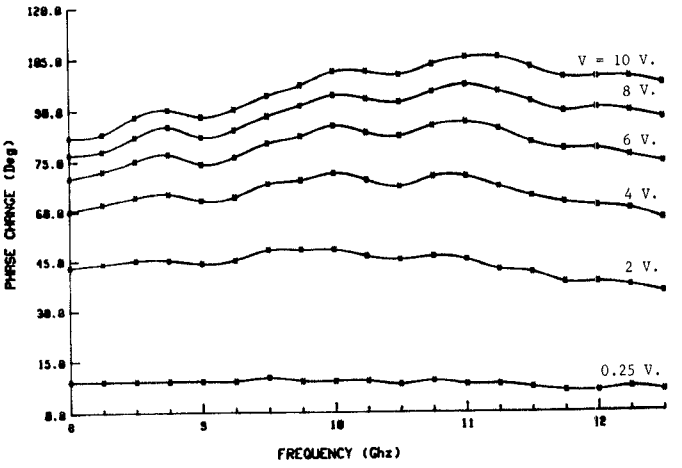


Fig. 9. Measured Phase Shift is flat with frequency. Varactors could be slightly forward biased to get more phase shift. Phase change is measured from zero bias.

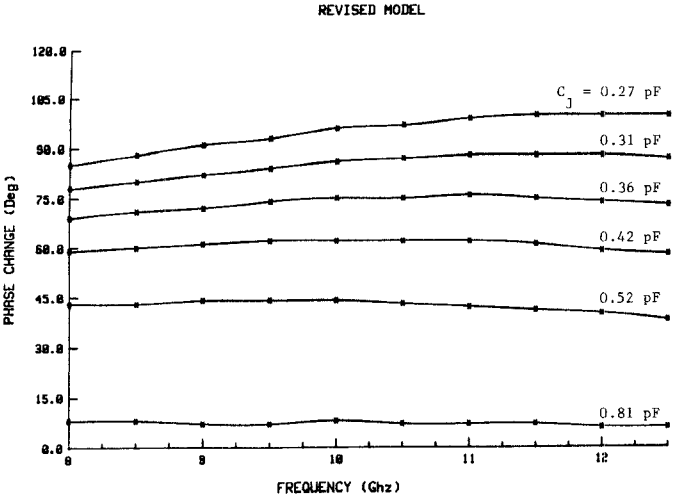


Fig. 10. To compare with the measured phase shift C(0) = 0.9 pF was substituted for expected value of 0.6 pF. Comparison is within 10^0. Phase change is calculated using zero bias as the reference state.

power levels and bias levels is shown in Figures 11 and 12. Deviation from small-signal performance at zero-bias (worse case) occurs at +12 dBm. The phase measurement is phase locked but not vector error corrected and has 5^0 of error. The measured device, because of the inductance of 0.6 nH and $C_j(0)$ of 0.9 pF, is resonant at 9.6 GHz where the circuit is most sensitive to change in capacitance. A 10% change in capacitance causes a 10^0 phase shift which is larger than that discussed above. A 0.4 V. peak RF voltage across each varactor corresponds to 8 dBm of input power. The phase shift variation at 5-10 dBm is about 1^0. With bias applied the power handling increases to 15 dBm (Fig. 12).

CONCLUSION

A 180° phase shifter has been designed and fabricated using Schottky varactor diodes hybrid-coupled and controlled by an analog voltage. The insertion loss has been minimized by choosing a 0.5-micron deep active layer for the surface oriented varactors. Phase shift variation with signal level is reduced by the use of series connected back-to-back varactors instead of single varactors. 105° of phase shift has been achieved experimentally with 0-10V. bias. If the measured diode capacitance is utilized in the circuit model, the measured and calculated phase shift agree within 10° and indicates the circuit works as expected. With further work 180° of phase shift can be obtained by reducing the anode area. The chip size is 0.077 x 0.100 inches (2 are required for 360°) and is 1/6 that of a 360° 4-bit switched-line phase shifter [4] (Fig. 13). The analog phase shifter offers a significant improvement for T/R module applications where the phase shifter chip is among the largest sized chips.

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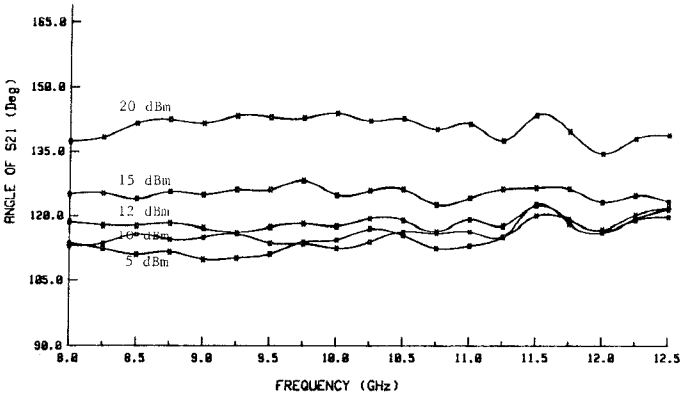


Fig. 11. Transmission Phase at Zero-Bias vs. Frequency. Deviation from small-signal occurs at 12 dBm.

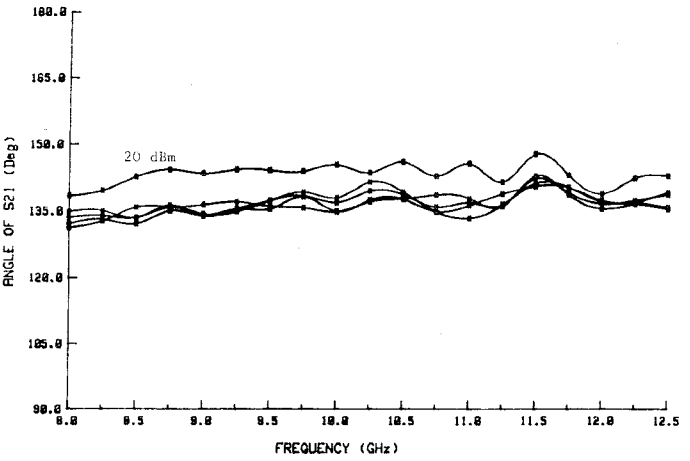
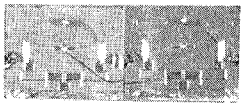


Fig. 12. Transmission Phase at 1.0V. Bias vs. Frequency. Deviation from small signal occurs at 20 dBm.



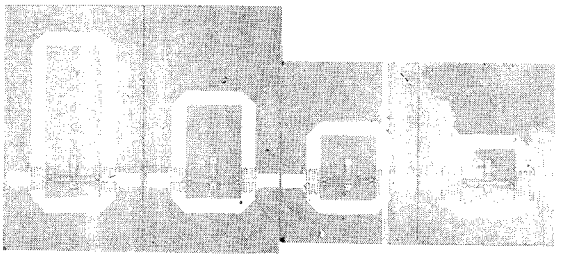


Fig. 13. The analog phase shifter (2 sections for 360°) is 1/6 the size of a switched-line phase shifter.